PVP 14

Code: EC5T5

III B.Tech - I Semester – Regular/Supplementary Examinations
October 2017

DIGITAL IC APPLICATIONS
(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11x 2 = 22 M

1.

a) Write down the gate-level Verilog code for a half adder.
b) What is meant by nesting? Is nesting of modules allowed in Verilog HDL?
c) Define register data type in Verilog HDL.
d) Which IC (logic family) is preferred for an application requiring high speed of access and to be performed consuming very less power. Does such IC possess high noise margin.
e) CD4001B is a name of a "Quad 2 input NOR gate". In this notation, what is meant by "Quad 2 input" ? What is the fan-in of this IC?
f) Write down the Verilog code for a 2x1 multiplexer, using if-else statements.
g) Draw the gate-level internal diagram of a 2 to 4 decoder.

h) Draw the block diagram of a mod-2 counter, using T flipflops.

i) Which shift registers are used for the purpose of multiplication and how?

j) What is non-volatile memory? State an example for a non-volatile memory element.

k) If a single 2 to 4 decoder is to used in design of a ROM, will there be any restriction/limitation of size of that ROM design?

PART – B

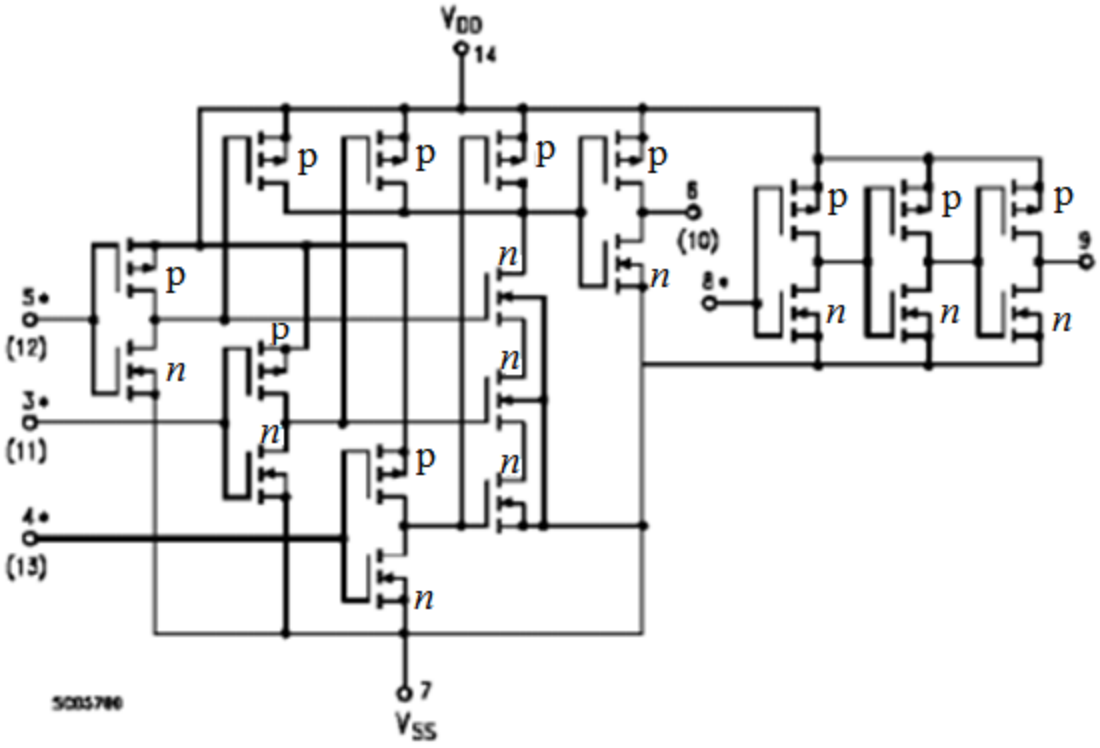
Answer any ***THREE*** questions. All questions carry equal marks. 3 x 16 = 48 M

2.a) Explain inter-assignment delay and intra – assignment delay with examples. 6 M

b) Advantages and disadvantages of behavioural modelling of Verilog HDL over structural modeling. 6 M

c) Define module instantiation and module instance in Verilog HDL. 4 M

3. The figure given below corresponds to a Quad 2-input NOR gate, identify the logic family it belongs (without getting into details of functionality) to and explain the questions/terms below with respect to that logic family: 2 M



a) t_{PLH} and t_{PHL} along with necessary waveforms. 5 M

b) Noise margin (V_{OH} , V_{IH} , V_{IL} , V_{OL}). 6 M

c) Logic levels. 3 M

4.a) Write down the truth table and expression for half adder and full adder. 4 M

b) Draw the block diagram of a 4 bit adder (Ripple Carry Adder) and explain its operation. 6 M

c) Write down the Verilog code for implementing above block diagram of 4 bit adder. 6 M

5.a) Design a sequential circuit for a frequency division by 10 ($f_{clk}/10$). 8 M

b) Write down a Verilog code for a D flip flop. 4 M

c) Write down a Verilog code for a Mod- 4 counter. 4 M

6.a) Discuss how PROM, EPROM and EEPROM technologies differ from each other. 8 M

b) Write down the applications of PROM, EPROM and EEPROM. 8 M